Low-Noise Amplifier with Wideband Feedforward Linearisation for Mid-Band 5G Receivers

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***Abstract*—This paper proposes a wideband linearisation technique for third-order intercept point (IP3) improvement in low noise amplifiers (LNAs). The proposed LNA is designed for mid-band 5G (3-4GHz) wireless receivers and it is based on a cascode topology. An auxiliary transistor provides a feedforward correction path for third-order intermodulation (IM3) cancellation. The effects of the second harmonic on the IM3 are also considered in the modelling. Theoretical and simulation analysis of the circuit result in a DC power consumption of 306mW from a supply voltage of 3V, an OIP3 of 30.8dBm, noise figure (NF) of 0.94dB and 13.8dB of power gain are obtained. The LNA is simulated for a hybrid circuit implementation using a 400um GaAs packaged transistor.**

***Index Terms*—Cascode, feedforward, fifth-generation (5G), linearisation, low noise amplifier, third-order intercept point (IP3), third-order intermodulation (IM3)**

I. Introduction

The mass deployment of wireless communication systems in the mid-band 5G frequencies results in high interference and this poses challenges on the linearity requirements of low-noise amplifiers (LNAs) across a wide range of frequencies [1]. Therefore, LNAs for sub-6GHz wireless receivers require high linearity across a wide range of frequencies to amplify wanted signals without distortion. The improvement in linearity should be achieved without compromising noise figure (NF) and gain [2].

Previous investigations propose feedforward linearity enhancement methods for cascode LNAs based on derivative superposition (DS) and modified DS topologies along with optimal biasing [1]–[4]. The DS topology employs two gate-connected transistors in common-source (CS), with one of them providing the feedforward correction path for cancelling the third-order intermodulation (IM3) products to improve the third-order intercept point (IP3). Modified DS, whilst relying on gate-connected transistors, also contributes in the mitigation of second-order nonlinearities in IM3 for a better IP3 improvement as compared to DS [4], [5]. However, the linearity improvement in these topologies is narrowband and restricted. To overcome this limitation, wideband DS (WBDS) cascode LNA has been proposed in [6]. Here, the modified DS with two gate-connected CS transistors is combined with a third auxiliary transistor for setting two input IP3 (IIP3) peaks in the band of interest, thus sustaining linearisation across a large bandwidth. However, WBDS, in addition to the auxiliary transistor for feedforward correction, still uses two gate connected CS transistors, degrading the NF and increasing power consumption.

In this paper, a modified WBDS (mWBDS) cascode LNA is proposed where the linearity enhancement technique of the modified DS cascode is merged with the wideband circuit design approach of WBDS. However, instead of two gate-connected CS transistors, only the auxiliary transistor is employed, improving power consumption and noise performance, whilst retaining the twin IP3 peaks required for wideband linearisation. Wideband noise reduction is also attained with inductive source degeneration, with the NF being comparable to the casocde LNA. In the following sections, the theory of mWBDS is first explained. This is followed by a theoretical analysis using the extended Volterra series for an analytical derivation of the IP3 peaks. Simulation results are then shown before concluding the paper.

II. Design and Analysis

The topology chosen for the LNA is the cascode with mWBDS feedforward correction for wideband IP3 improvement. The schematic is shown in Fig. 1. It consists of the CS and common-gate (CG) transistors M_{cs} and M_{cg}, respectively. The auxiliary transistor M_{aux}, also in CS, and in parallel with M_{cs}, provides the feedforward correction path for wideband cancellation of IM3 terms at the source of M_{cg}. Transistor M_{diode}, configured as a diode connected load to M_{aux}, in conjunction with bias V_{aux}, maintains the operation of M_{aux} within an optimal region such that the wideband cancellation of the third derivative terms $g_{3,cs}, g_{3,aux}$ of M_{cs}, M_{aux} respectively, is achieved. The resistors R_{bias} block the effect of RF signals on the bias. The tank circuit C_t, L_t resonates with the output match to provide gain across the band. Other capacitors function as DC blocks, bypass and coupling.

A. Linearisation with mWBDS

In common DS techniques, an amplifier in CS configuration is connected in parallel with an auxiliary amplifier biased optimally such that they have opposite $g_{3,cs}$ and $g_{3,aux}$ [2], [5].

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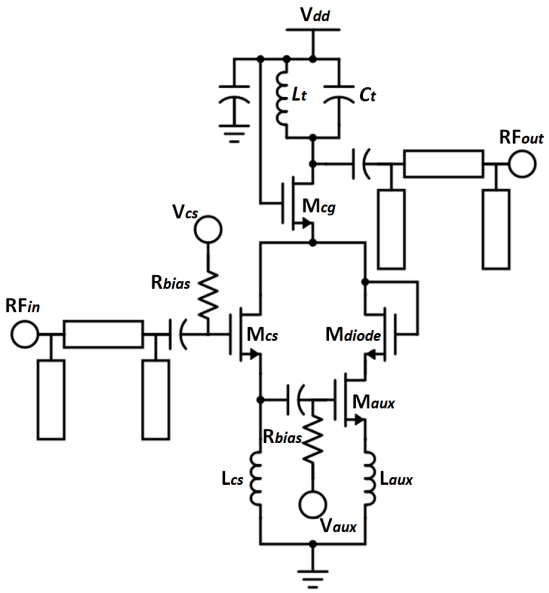

Fig. 1. Schematic of the proposed cascode LNA with feedforward correction path.

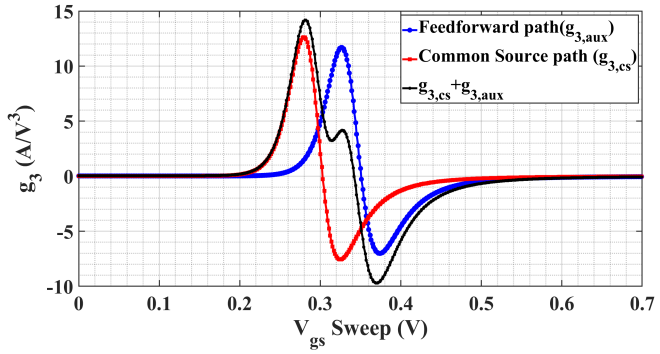

Fig. 2. Third derivative terms of the CS amplifier ($g_{3,cs}$) and the auxiliary amplifier ($g_{3,aux}$), vs. V_{gs} of both M_{cs} and M_{aux}.

Here, the CS amplifier has the negative peak of its $g_{3,cs}$ aligned with the positive peak of $g_{3,aux}$ of the auxiliary amplifier, so as to attain the maximum possible cancellation of IM3 terms, that results in improved IP3. However, the main drawback here is the trade-off of wideband IP3 enhancement with NF. The auxiliary amplifier adds to the existing gate induced noise power of the CS amplifier, given by [7]

$$\overline{i^2_{ng,DS}} \approx \frac{4}{5}\frac{kT\delta\omega^2(C_{gs,cs}+C_{gs,aux})^2\Delta f}{(g_{m,cs})} \tag{1}$$

where T is the temperature, k is the Boltzmann constant, δ is the gate noise coefficient, ω is the angular frequency, Δf is the noise bandwidth in Hertz, C_{gs} is the gate-to-source parasitic capacitance, and g_m is the transconductance, and the subscripts $_{cs}$ and $_{aux}$ denote the transistors M_{cs} and M_{aux}, respectively. Furthermore, as can be observed in (1), M_{aux} loads the input of M_{cs} by adding an extra capacitance. This exacerbates the noise performance, detunes the input impedance and reduces the frequency of operation. Wideband linearity can therefore be achieved without degrading the noise performance only if

i. the auxiliary amplifier does not degrade the gate induced noise of the CS amplifier,
ii. the contribution of second-order nonlinearity to IM3 components is taken into account, and,
iii. (i) and (ii) are merged with wideband circuit design techniques to sustain linearity enhancement across wide bandwidth.

The second harmonics $(2\omega_{1,cs}, 2\omega_{2,cs})$ generated at M_{cs} due to second-order nonlinearity are fed back through the gate and source of M_{cs} and mix with the fundamental components. This results in IM3 components at $2\omega_{1,cs}\pm\omega_{2,cs}$ and $2\omega_{2,cs}\pm\omega_{1,cs}$. In this way, the second harmonics contribute to IM3, and a corresponding relationship for IIP3 is derived as [4]:

$$\text{IIP3} = \frac{4g^2_{1,cs}\omega^2 L_{cs}C_{gs,cs}}{3\left|g_{3,cs} - \dfrac{2g^2_{2,cs}/3}{g_{1,cs} + \dfrac{1}{j2\omega_{cs}L_{cs}} + j2\omega_{cs}C_{gs,cs} + Z_{s,cs}(2\omega)\dfrac{C_{gs,cs}}{L_{cs}}}\right|} \tag{2}$$

where $Z_{s,cs}$ is the input impedance of M_{cs}. (2) implies that a zero $g_{3,cs}$ does not by itself result in high IP3 due to a non-zero $g_{2,cs}$. However, despite this limitation, (ii) can be largely accomplished by drawing the input of the auxiliary amplifier M_{aux} from the source of the CS amplifier M_{cs}, as shown in Fig. 1. This is because the drain current of M_{cs} contains the IM3 components generated due to third-order and feedback of second harmonics. Hence, connecting the gate of M_{aux} to the source of M_{cs} captures the IM3 information present in the drain current of M_{cs}. Moreover, when biased optimally, M_{aux} can process information present in the drain current of M_{cs} to generate an output current with its IM3 components (due to $-g_{3,aux}$ of M_{aux}) equal in magnitude and opposite in phase with that of M_{cs} (due to $+g_{3,cs}$ of M_{cs}), as shown in Fig. 2. This achieves the objective in (ii), resulting in minor IM3 current at the input of the CG amplifier M_{cg}. Furthermore, the source degeneration inductors L_{cs} and L_{aux} act as frequency dependent negative feedback to M_{cs}. They provide a feedback factor of $\beta = \omega(L_{cs}+L_{aux})$, reducing the capacitve reactance of C_{gs} and C_{aux} thus lowering the gate induced noise power given by (1). In this way, (i) is fulfilled.

In order to achieve (iii), noise reduction and linearity enhancement techniques in (i) and (ii) are combined with wideband circuit design methods. This is represented in Fig. 3. Essentially, the aim is to obtain two output IP3 (OIP3 (=IIP3$+G_T$), G_T : transducer power gain) peaks, one each at lower and upper edges of the band as shown in Fig. 4, in order to sustain an overall IP3 improvement across the band. Whilst in the previously proposed WBDS technique [6], two gate-connected CS amplifiers set the lower frequency OIP3 peak (with one of them the main and the other the feedforward), a wideband technique using an additional auxiliary amplifier sets the upper frequency OIP3 peak. However, the drawback here is the use of three transistors (two gate-connected and

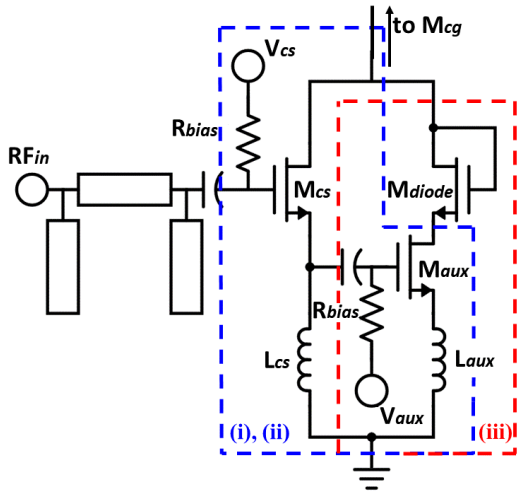

Fig. 3. Cascode with mWBDS feedforward showing the merging of (i) noise reduction and (ii) linearity enhancement technique (iii) wideband circuit design approach for sustaining IP3 improvement across a wide bandwidth.

one auxiliary). The use of three transistors results in higher power consumption and degrades NF. Moreover, employing two transistors for feedforward correction is a redundancy. Hence, in our proposed topology of mWBDS, we remove the redundant gate-connected transistor, choosing to retain only the auxiliary M_{aux} (for feedforward correction) as shown in Fig. 3. This is sufficient for achieving IM3 cancellation through optimal biasing ($+g_{3,cs}$, $-g_{3,aux}$) whilst reducing the contribution of second-order nonlinearities in IM3. The former sets the lower OIP3 peak whilst the latter sets the upper OIP3 peak, which achieves wideband linearisation in our proposed mWBDS topology.

B. Extended Volterra Series Analysis

An approximate IIP3 expression for the mWBDS topology is derived based on previous investigations in [2], [6] as

$$\begin{aligned}\text{IIP3} =& \frac{4g_{1,aux,HB}^2\omega^2\left[L_{cs}(C_{cs}+C_{aux})+C_{aux}L_{aux}\right]}{3|\epsilon|}\\ \epsilon =& g_{3,aux,HB}-\frac{g_{2,aux,HB}^2}{3g_{1,aux,HB}}+\\ &\left[1+\frac{L_{aux}(C_{gs,aux}+j\omega g_{1,aux,HB}C_{gs,cs}L_{cs})}{L_{cs}(C_{gs,cs}+C_{gs,aux})+C_{gs,aux}L_{aux}}\right]\cdot\\ &\{g_{3,cs,HB}\left[1+j\omega g_{1,aux,HB}L_{aux}\right]+\\ &j\omega g_{1,aux,HB}L_{aux}\left[g_{3,cs,HB}+\omega^2 g_{1,aux,HB}^3L_{aux}^2\right]\},\end{aligned} \tag{3}$$

where the new set of coefficients $g_{k,aux,HB}, g_{k,cs,HB}|k \in \{1,2,3\}$ are known as the extended Volterra coefficients [6]. Extracted from two-tone Harmonic Balance (HB) simulations, these coefficients are classified at each output frequency where IM3 products are generated, and are defined as the ratio of the AC drain current to the AC gate-source voltage at each output frequency. They are computed as follows [6]

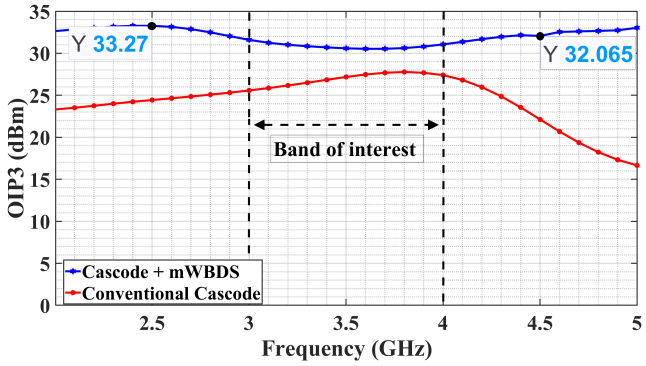

Fig. 4. Wideband linearisation in the mid-band frequencies due to two distinct OIP3 peaks towards the band-edges (2.5GHz and 4.5GHz).

$$\begin{aligned} g_{1,cs,HB,f_1} &= \frac{i_{d,cs,HB,f_1}}{v_{gs,cs,HB,f_1}},\\ g_{3,cs,HB,2f_1-f_2} &= \frac{i_{d,cs,HB,2f_1-f_2}}{v_{gs,cs,HB,2f_1-f_2}};\\ g_{1,cs,HB} &= \frac{g_{1,cs,HB,f_1}+g_{1,cs,HB,f_2}}{2},\\ g_{3,cs,HB} &= \frac{g_{3,cs,HB,2f_1-f2}+g_{3,cs,HB,2f_2-f_1}}{2};\end{aligned} \tag{4}$$

where i_{d,cs,HB,f_1} is the AC drain current of M_{cs} at f_1 and v_{gs,cs,HB,f_1} is the corresponding gate-source voltage at f_1 with the subscript $_{HB}$ denoting HB simulation. The second-order coefficients for M_{cs}, and, the coefficients for M_{aux}, are also similarly derived. The extended Volterra coefficients can be tuned to obtain high OIP3 by choosing the optimal values of L_{cs} and L_{aux}. Fig. 5 shows the theoretical values of OIP3 in a MATLAB™ simulation for the computed values of extended Volterra coefficients derived by using the procedure in (3) and (4), with fixed values of $C_{gs,cs}$ and $C_{gs,aux}$, at the centre frequency of 3.5GHz. It is observed in Fig. 5 that the values of the OIP3 at the output frequency, arrived at through the analytical procedure, are a close match with the OIP3 obtained in Fig. 4. Therefore, the theoretical analysis of the extended Volterra series validates our simulation results.

III. Simulation Results

The results in this section are obtained using the ATF-55143 GaAs pHEMT transistor model in Keysight™ Advanced

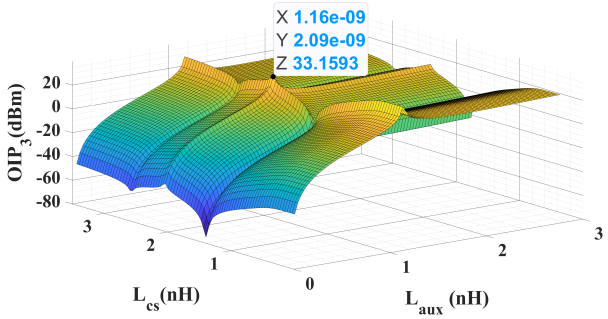

Fig. 5. MATLAB™ simulation showing OIP3 obtained from the theoretical analysis of extended Volterra series coefficients.

TABLE I
NF, G_T AND OIP3 COMPARISON AT MID-BAND 5G FREQUENCIES

	Freq (GHz)	NF (dB)	G_T (dB)	OIP3 (dBm) RF spacing 0.25GHz	OIP3 (dBm) RF spacing 0.5GHz	OIP3 (dBm) RF spacing 0.75GHz	OIP3 (dBm) RF spacing 1GHz
Cascode with mWBDS feedforward	3	0.8	14.7	29.4	30.8	32.5	34.2
	3.5	0.9	13.8				
	4	1.2	12.2				
Cascode	3	0.7	13.2	25.8	26.1	25.8	25.0
	3.5	0.8	13.3				
	4	1.0	11.3				

Design System™ (ADS™). Fig. 6 presents the S-parameters of the proposed topology with a frequency sweep from 2GHz to 5GHz. The S21 shows a gain between 12.2dB and 14.7dB within 3-4GHz interval. The input and output reflection coefficients (S11, S22) are below 10dB in the band of interest. The linearity analysis employs a two-tone test signal with RF spacings of 0.25GHz, 0.5GHz, 0.75GHz and 1GHz, in a HB simulation using the transistor nonlinear model to demonstrate the wideband nature of the LNA. The illustration of IP3 of the proposed mWBDS in comparison with the traditional cascode is shown in Fig. 7 for 0.5GHz RF spacing. The mWBDS achieves wideband linearisation with over 4dB higher OIP3 than the conventional cascode. The proposed topology shows a slight increase in the NF of about 0.1dB in comparison with the cascode, Fig. 8, but with the benefit of a higher OIP3, as summarised in Table I.

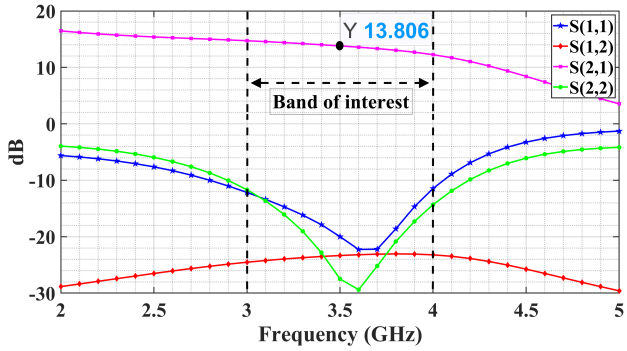

Fig. 6. Scattering parameters for mWBDS

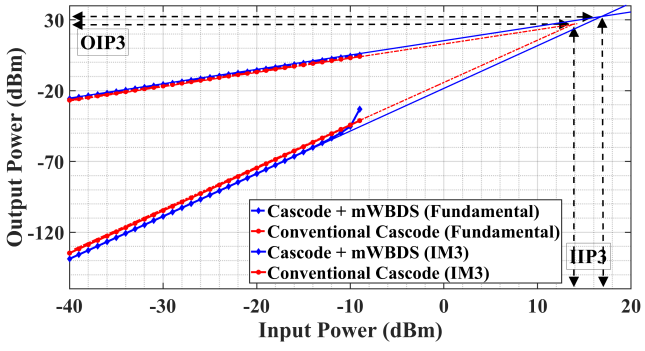

Fig. 7. Fundamental and IM3 curves in a P_{in} vs. P_{out} sweep with the respective third-order intercept points (IP3) for mWBDS vs. cascode.

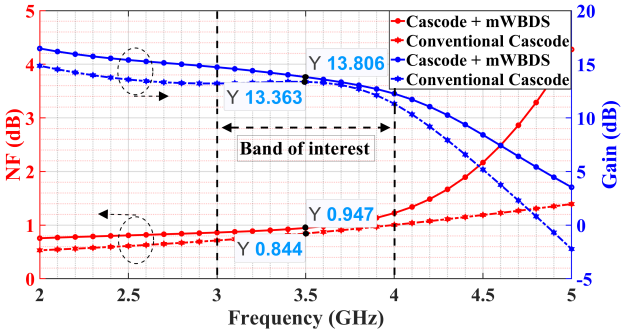

Fig. 8. Comparison between the gain and the noise figure (NF) for mWBDS vs. cascode.

CONCLUSION

In this paper, mWBDS cascode LNA is proposed for wideband linearisation at mid-band 5G frequencies. The mWBDS merges linearity enhancement techniques with a wideband circuit design approach, to set two OIP3 peaks at the band-edges which sustains a high linearisation across a wide frequency range. Theoretical analysis using the extended Volterra series confirms the OIP3 improvement and validates our simulation results. By applying the mWBDS feedforward technique, over 4dB of linearity improvement is observed at 3.5GHz as compared to the conventional cascode, power gain of 13.8dB and NF of 0.94dB.

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